Development of a Silicon-based Single Electron Transistor

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Single electron transistors (SETs) are of great interest for future nanoelectronic circuits [1] due to their small size, low power consumption, and ability to perform fast and sensitive charge measurements [2]. Silicon SETs in particular are advantageous since they have been shown to operate with remarkable stability [3], and they may be fabricated using techniques which are compatible with conventional integrated circuit technology.

The silicon SET studied in this work is designed for controllable and reproducible low temperature operation. It comprises a dual gate structure on a silicon-on-insulator substrate. A silicon quantum wire is formed in a high-resistivity superficial silicon layer using reactive ion etching. Carriers are induced in the silicon wire by utilizing the low-resistivity silicon substrate as a back gate, which is separated from the superficial silicon by an ∼80 nm thick buried oxide. The tunnel barriers are created electrostatically, using lithographically defined metallic electrodes (∼40 nm width). These electrodes surround the quantum wire, producing strong electrostatic confinement. This architecture provides independent control of tunnel barrier height and island occupancy, thus permitting excellent control of Coulomb blockade oscillations, as has been shown recently in a similar device [4]. The tunnel barrier gates also allow silicon quantum dots to defined electrostatically within the silicon wire. A schematic of the device is shown in Figure 2(a).

The use of the SOI substrate as a back-gate has been demonstrated in double-gated MOSFETs and in silicon wires. The double-gated MOSFETs were fabricated with a superficial silicon thickness of approximately 100 nm. Hall measurements performed on these devices confirmed the formation of two inversion layers, which were independently controllable by the top and back gates of the device. The results of these Hall measurements are shown in Figure 1. Preliminary measurements carried out on 50 nm thick, 1 μm wide silicon wires confirm the control of carriers in the superficial silicon by the back-gate, as seen in Figure 3. Silicon SETs, including gates for electrostatic tunnel barrier control, are currently in fabrication. An SEM image of one of these devices is provided in Figure 2(b). Latest results will be presented at the conference.

[1] K.K. Likharev, *Proceedings of the IEEE* **87**, 606 (1999).
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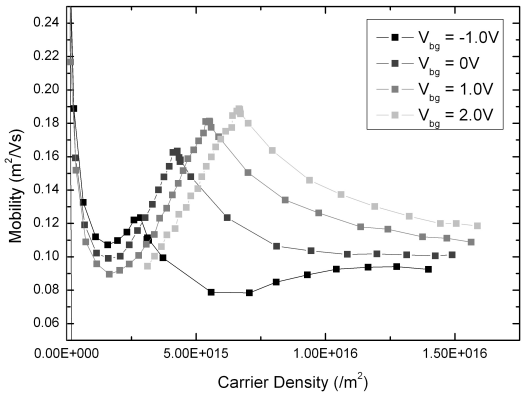
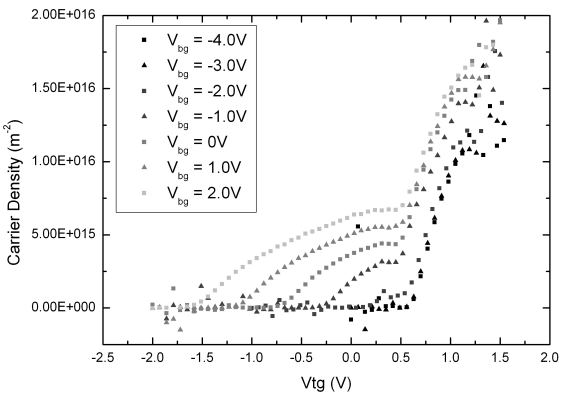
[3] N.M. Zimmerman, W.H. Huber, A. Fujiwara and Y. Takahashi, *Appl. Phys. Lett.* **79**, 3188 (2001).
[4] A. Fujiwara, H. Inokawa, K. Yamazaki, H. Namatsu, Y. Takahashi, N.M. Zimmerman and S.B. Martin *Appl. Phys. Lett.* **88**, 053121 (2006).

Figure 1: Results from Hall measurements taken on a double-gated SOI MOSFET at 4 K

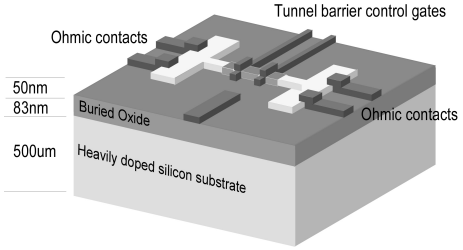


(a) Mobility as a function of carrier density

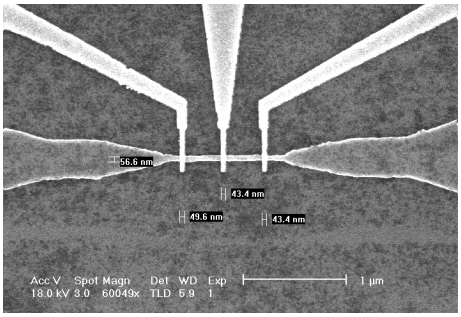


(b) Carrier density as a function of applied top-gate voltage

Figure 2: Silicon SET



(a) Schematic diagram of the Si SET studied in this work.



(b) SEM image of an Si SET in fabrication.

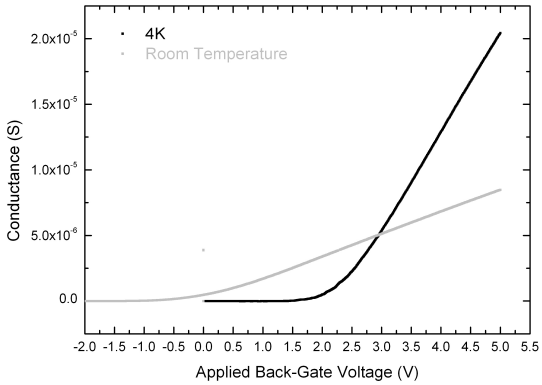


Figure 3: Conductance of a 50 nm thick, 1 μm wide silicon wire as a function of applied back-gate voltage.