Nanostenciling and Pulsed Laser Deposition: a Versatile Combination for Parallel Patterning and Prototyping of Functional Materials

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Research in semiconductor physics is continuously motivated by the aim of improving device performance, which typically translates into increasing the density of the integrated individual components by decreasing their size. For most applications, nanostructure fabrication is the foremost challenge. In this context top-down and bottom-up fabrication approaches are both being explored to tailor structures at the nanometer scale and to pattern them in a desired fashion [1].

The trend towards device miniaturization has been sustained so far by the constant development of advanced optical lithography for parallel large scale production. For serial, small scale patterning, electron-beam lithography has been proposed as the technique of choice as it is capable of providing the best feature resolution. However, for this technique, production costs become formidable for surface patterning in the nanometer range.

Unconventional patterning approaches have emerged as low–cost, high–resolution alternatives to optical projection lithography. An important approach in this field falls into an area known as "soft lithography" (e.g. μ-contact printing, replica molding). Significant advances in defining nano-patterns have been made by nanoimprint lithography (NIL) as well as by its related variant, step and flash imprint lithography (S-FIL) both showing great potential for the semiconductor industry. All these techniques are based on the mechanical transfer of a pattern from an elastomeric stamp or a hard mold to the substrate by direct contact.

The common drawback of these alternative solutions, as well as of all lithographic approaches, is that they require resist or polymer processing and consequently many chemical, thermal and etch associated steps. Thus, the ability to fabricate arrays of structures with controlled size and shape, with limited interaction with the substrate of choice and using a minimal number of processing steps, is an ongoing challenge in nanotechnology.

Controlled deposition through a miniature shadow–mask or nanostenciling has been recently revisited and considered as a suitable method to grow directly patterned nanostructures, in a single step, either in dynamic or static modes [2], [3]. While offering unlimited freedom in choosing the physical vapor deposition method, pattern formation using nanostencils turned out to be a straightforward, low–cost and reliable method. Moreover, it drastically reduces the number of processing operations with respect to resist–based lithography.

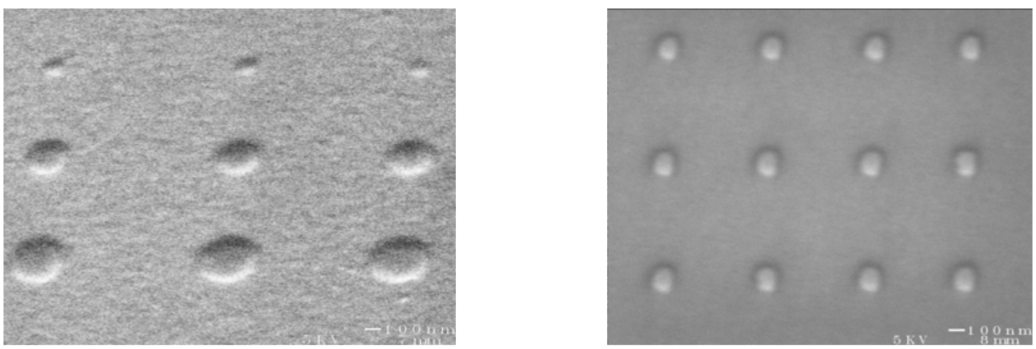
This approach that we are currently expanding on and investigating in detail is in principle directly applicable to the deposition of any material on any substrate [4], [5]. We will describe our recent work on the fabrication and patterning of three major classes of materials, namely metals (e.g. Pt, Cr), semiconductor hetero–structures (Ge/Si) and complex functional oxides (ABO_3 perovskite-type ferroelectrics) by nanostenciling and pulsed laser deposition (PLD). PLD emerged as a convenient deposition method because of its high versatility in growing stoichiometric thin films on a wide range of substrates. Moreover it offers the possibility of fine-tuning and controlling deposition parameters and therefore, the properties of the films and structures.

The combination of stenciling and PLD allows for the accurate organizing of structures into desired architectures. Selective deposition is obtained by interposing a sieve with apertures down to 100 nm between source and substrate. And, the material deposited through the stencil mask conserves the desired functionality even at the level of the individual nanostructures (e.g. piezo and ferroelectricity at the nanoscale proven by piezoresponse force microscopy (PFM)).

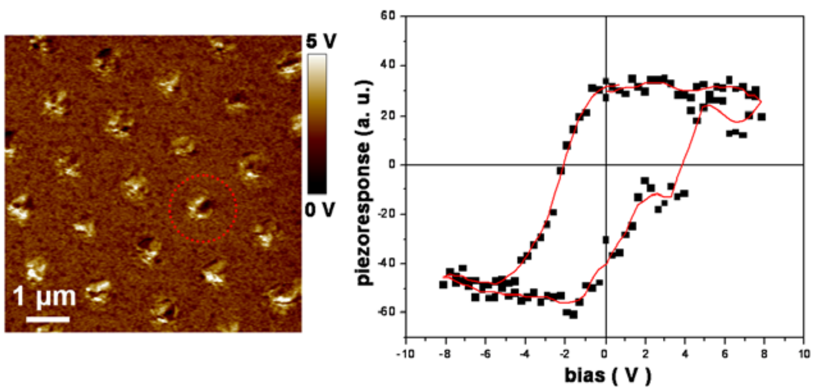
We will also discuss the application of a nanoscale multi-level-stenciling approach which may enable rapid prototyping of functional heterostructures composed of stacks of different materials (e.g. metal-oxide-metal and multiferroic structures grown by sequential depositions). The morphology and composition of theses nanostructures were characterized by SEM, AFM, XRD and XPS techniques and their local ferroelectric properties were detected using PFM.

The application of this process is meant for research (e.g. studying the size effects on the functional properties of the structures) but also represents a promising universal “tool” for parallel deposition of high-resolution and purity nanostructures of functional materials under high and ultra-high vacuum. Nanostenciling can be performed under these controlled conditions and is suitable for parallel prototyping of fragile or functionalized surfaces. Further developments of this approach are expected to lead to novel architectures and devices, also providing solutions for critical patterning issues not yet solved.

[1] C.V. Cojocaru, F. Ratto, C. Harnagea, A. Pignolet and F. Rosei, Microelectron. Eng. 80, (2005), 448
[2] J. Brugger, J.W. Berenschot, S. Kuiper, W. Nijdam, B. Otter and M. Elwenspoek, Microelectron. Eng. 53, (2000), 403
[3] R. Luthi, R.R. Schlittler, J. Brugger, P. Vettiger, M.E. Welland, and J.K. Gimzewski, Appl. Phys. Lett.75, (1999), 1314
[4] C.V. Cojocaru, C. Harnagea, F.Rosei and A. Pignolet, M. van den Boogaart, J. Brugger, Appl. Phys. Lett86, (2005), 183107
[5] C.V. Cojocaru, C. Harnagea, A. Pignolet and F. Rosei, IEEE, Transactions on Nanotechnology, (2006), in press



SEM micrographs of ordered Ge structures (100-350 nm in width) on Si(100) (left) and $BaTiO_3$ structures (125 nm in width) on Nb doped $SrTiO_3$ (100) oriented substrates (right) deposited at room temperature



Piezoresponse domain image (left) of patterned ferroelectric $BaTiO_3$ on 0.1% Nb doped $SrTiO_3$ and piezoresponse hysteresis loop obtained from an individual structure