NANOSTRUCTURED POROUS SILICON AS THICK ELECTRICAL INSULATOR FOR RF APPLICATIONS

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Porous silicon (PS) is a promising material for electronics and sensors devices. This material exhibits attractive properties [1-3] such as quantum confinement (silicon based photo-emitting devices), a large specific surface (chemical sensors) and insulating potentialities. As illustrated in figure 1, Meso-porous form (crystallites size around 10_/100 nm) presents columnar structure allowing thick and mechanically stable porous layer production. It is known as an electrical semi-insulator even at low porosity [4-6]. The residual electrical conduction of the porous layers is due to various electrical transport mechanisms: quasi intrinsic conduction within continuous paths of nano-crystallites at low frequencies, Space Charge Limited Currents under DC voltage bias and hopping transport on localized states in the chaotic porous structure at high frequencies. So, the electrical insulating capabilities of this material need an accurate evaluation considering the conditions of use (thickness, electrical bias, temperature, frequency,...).

In the present work, our study concern non biased thick meso-porous silicon layers with the aim of rf devices integration which require efficient thick insulating substrates. In these conditions, the electrical transport in the layers is controlled by the intrinsic and hopping bulk conduction. We have used complex impedance measurements and rf resonant circuits characteristics to determine the electrical parameters of spiral inductors /porous-Si/Si structures (see figure 1). The samples were realized on $10^{-2} \Omega$ -cm p-type Si substrates using a well known anodic electrochemical dissolution process [7] to etch porous layers of 100µm of thickness and 50% of porosity. The impedance of the porous layers is determined in $10^2 - 10^6$ frequency range from measurements between the metallic inductor (used as an electrode) and the P⁺ substrate using a HP 192 bridge in parallel mode.

As shown in figure 2, at different temperatures, for frequencies higher than 100 kHz, the capacitance part of the impedance corresponds to the geometrical value and remains constant when the conductance part increase with the frequency revealing a hopping conduction phenomena. However, the tangent loss value is 10^{-2} at 100 kHz and decreases with the frequency. This indicates clearly the capacitive nature of porous silicon at high frequencies. Rf measurements on the corresponding resonant circuit are reported below on figure 3 using the integrated inductor with external capacitance. The measurements were carried out using an Agilent E5070B network analyzer in S₁₁ parameters mode (figure 3a). The extracted loss resistance is compared to numerical data obtained by mean of Femlab software simulations. We can see from a typical curve on figure 3b that moderately oxidized porous silicon exhibits a comparable value of loss resistance than efficient insulators such as glass or vacuum in a prospected frequency range of 10^5 Hz to 10^9 Hz.

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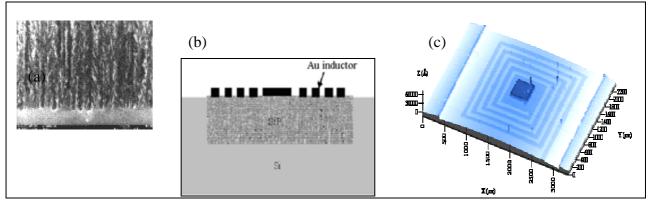


Fig. 1. Geometrical configuration of the samples: (a) morphology from cross-section SEM view (b) Au inductor /PS/p_-Si structures; (c) view of 2mmx2mm microcoils.

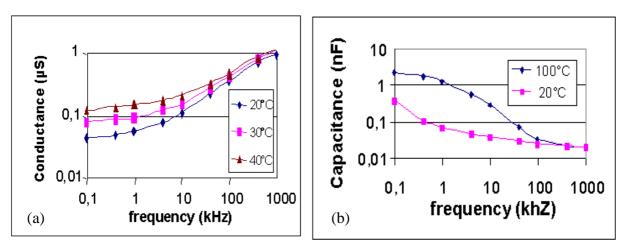


Figure 2. (a) conductance – frequency and (b) capacitance – frequency measurements of the porous layers at different temperatures.

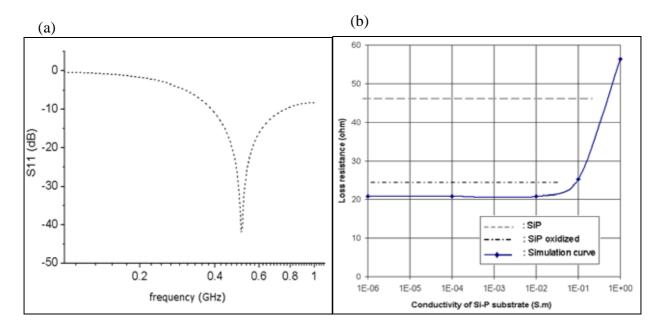


Figure 3. (a) typical spectra of the resonant circuit (b) simulated loss resistance variation with the dielectric conductivity (dashed lines: experimental data using porous silicon dielectric)