NANO FABRICATION OF FinFETS TO FORM NANO SCALED INTEGRATED CIRCUIT CHIPS

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ABSTRACT

Semi-conducting, metallic and insulating nanowires are today's building blocks in nanotechnology. Due to their small size, anisotropy and cost effectiveness it is viable to integrate Nano scaled elements into Nano IC chips. Strategies have emerged to position nanowires and Nano circuits on substrates to allow integration of Nano electronic devices. In this paper we describe the fabrication and assembly of Nano devices to form functional IC chips on a nanometer scale. Several methods have been developed from nanofabrication based on self-assembled alumina templates, using biomolecules for self-assembly of engineered Nano-scale devices and Nano structuring of ceramic surfaces by ways of unconventional lithographic methods, electron beam induced deposition, electron-ion beam lithography and electron beam direct writing[3].

We will begin by a review of the basic structure of IC chips and their varying properties using different materials and then move on to how these properties differ at a Nano scale. Hence we will describe how the basic components such transistors (FinFETs) can be engineered using various lithographic and non-lithographic methods. Hence implementing a majority gate and a 2-1 MUX by using both gates of FinFET[2] transistors as inputs is presented. Simulation results show that FinFET logic implementation has significant advantages over static CMOS logic and pass transistor logic in terms of power consumption and cell area therefore aiming at the end result which includes Nano-scaled IC chips which provide optimum efficiency and are cost effective[1].

KEYWORDS

Nano-scaled IC chips, nanofabrication, nanowires, lithographic methods, semiconductor quantum dots, electron-ion beam, metal dot array, ceramic surfaces, biomolecules, alumina templates, optimum efficiency, cost effective.

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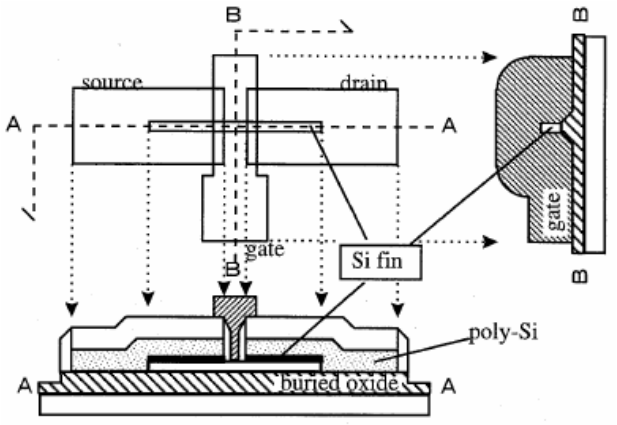

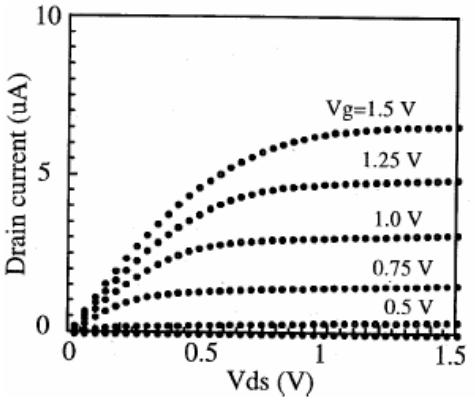

Fig 1(a) : Schematic of nano fabricating FinFETS with double fin gates.
Fig 1(b) : Graph of drain current vs the drain source voltage.