Keynote

SEMICONDUCTOR NANOWIRES FOR EMERGING NANOELECTRONICS APPLICATIONS

Lars Samuelson
Lund University, Solid State Physics / the Nanometer Structure Consortium
Box 118,S-221 00 Lund, Sweden
lars.samuelson@ftf.lth.se

Nanowire technology allows a bottom-up approach towards fabricating extremely small devices with negligible surface damage and with very high materials quality. The control of position, dimensions and formation of abrupt heterostructures will be described and examples of electronic and photonic devices created by this approach will be given.

Many applications based on bandstructure and/or heterostructure engineering would benefit if lateral confinement to one-dimensional (1D) systems could be achieved. Obvious examples are photonic structures where the shape of a pillar is defining a designed optical cavity. Other advantages may be related to designed electronic and photonic properties, leading to suppression of carrier scattering or to specific optical transition rules and polarization. For electronics and photonics, the reduction of device dimensions to 1D and 0D is the natural limit for a general trend in miniaturization, a limit where lateral quantization occurs and fully quantized systems may be obtained. In this talk I will give an update of the status of the field of self-assembled and epitaxially nucleated semiconductor nanowires.

Based on highly advanced epitaxial growth methods, such as MBE and MOVPE, stacked planar layers can be grown and be used to define heterostructure-defined vertical structures [1, 2]. If such structures are further processed via top-down patterning and etching, 1D and 0D hetero-structure systems can be realized, however with properties in most cases dominated by process-related damage. This is a reason why great efforts are made in developing techniques by which ultra-narrow (down to about 5 nm) nanowire device structures can be formed via self-assembly, by which the narrow structures are structurally ideal out to the very surface layer. The method used is described as the vapor-liquid-solid (VLS) growth mode, with the interface between the particle/droplet is the catalytic spot where growth is induced. I will in the first part describe the growth method and will present recent observations suggesting that in many cases growth occurs from a metallic particle in the solid phase, which would make growth a vapor-solid-solid (VSS) growth mode [3]. I will describe the status of technology for lithographic control of position as well as dimensions of nanowires [4], as well as opportunities to grow device-quality III-V nanowires on silicon substrates [5]. Of special interest is the possibility to form heterostructures between different materials within a nanowire, with abruptness on the atomic scale, of interest for basic low-dimensional physics as well as electronic and photonic devices [6].

So far, most of the devices [7] that we have realized and studied so far are really devices for physics studies, based on single-electron transistor phenomena, on resonant tunnelling effects or on the studies of few-electron phenomena in quantum dots formed in nanowires [8], all studied via tunnelling through a quantum dot via thin tunnelling barriers. I will report on the realization of NW devices of relevance for single/few-electron storage applications [9], for vertical wrap-gate field-effect transistors [10] and highly perfect core-shell nanowires [11].

Finally, I will give a brief update on the progress within the EU-funded Integrated Project NODE (Nanowire-based One-Dimensional Electronics).

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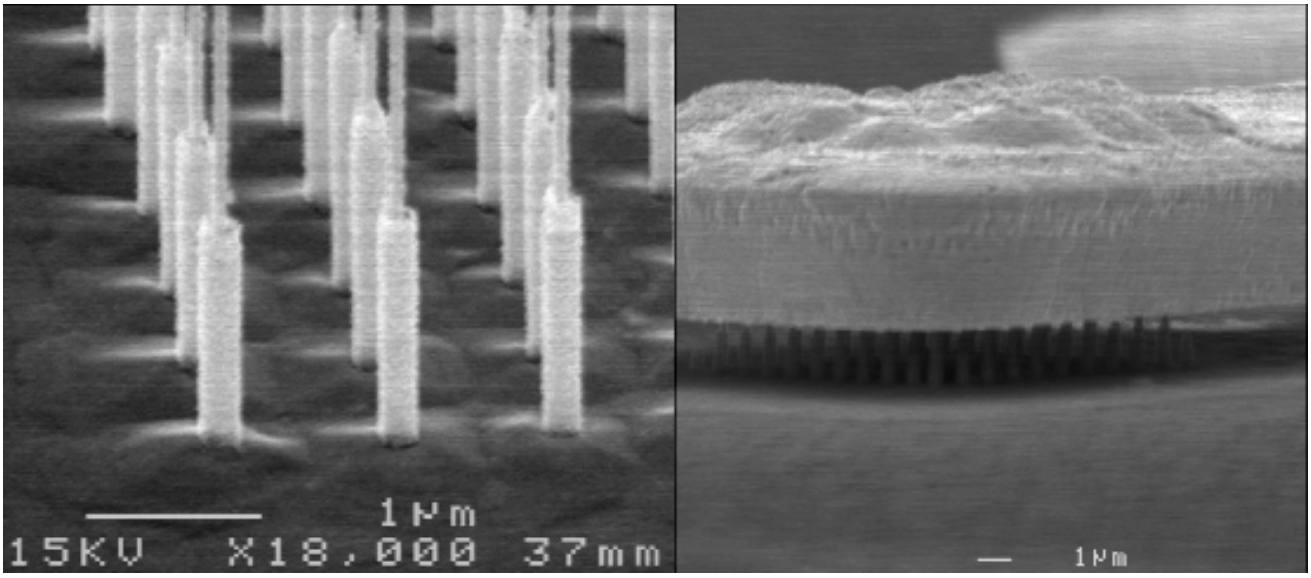
Figures:



Examples from the recently developed technology for formation of parallel arrays of three-terminal wrap-gate InAs field-effect transistors. The left image is an SEM-image of a lithographically defined 2D array with lower segment of wrap-around dielectric + gate visible. The right-hand image shows the finished device structure where many (e.g. 100) identical wrap-gate FETs are connected to common drain (top contact) and wrap-gate. For details, see Ref. 10.