

## COMPUTING AT THE NANOSCALE

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There is currently a tremendous business incentive to invent new electronic devices and circuits that will have dimensions of the order of nanometers. In addition, new fabrication techniques will be required that can inexpensively produce and connect these devices in vast quantities. The challenges are equivalent to those faced by the inventors of both the transistor and the integrated circuit, who replaced the existing vacuum-tube and wiring technologies with solid-state switches and lithographic fabrication, respectively. In order to satisfy these challenges, we have assembled a trans-disciplinary team of chemists, physicists, engineers, computer scientists and mathematicians at HP Labs to work simultaneously on the architecture, device physics and manufacturing chemistry of nanoscale circuits. The intention of this research is to complement and extend CMOS technology for as long as possible, and to replace transistors when necessary.

Two complementary research areas relevant to future nanocomputing systems are currently under investigation: (a) nano-scale electronic switching devices [1] and circuits [2], and (b) the development of new and inexpensive fabrication techniques [3]. Our approach for the construction of nanoelectronic circuits involves the explicit incorporation of defect tolerance [4], which is the capability to operate perfectly even in the presence of manufacturing mistakes in the circuit, into the design of the system. This prerequisite arises from the realization that it is prohibitively expensive to fabricate a perfect network of billions of nanoscale components. However, by introducing the appropriate amount of redundancy and utilizing concepts from coding theory [5], arbitrary complexity can be programmed into a highly regular structure and at the same time any defects can be mitigated.

Our research group has recently demonstrated the ability to fabricate electronic devices with sub-viral length scales (e.g. ~15 nm) [6] and to build nanoscale devices with the capability to perform signal restoration and inversion [7] (required for universal computing) without the need for transistors or any semiconductor at all. This has led us to understand that there are other computationally complete logic families besides NAND and NOR that are specifically suited to the properties of nanoscale switches and crossbars. We have built and demonstrated memory and logic circuits based on these new ideas that dramatically exceed the density of today's semiconductor circuits.

I will describe how fundamental research in a corporate research laboratory can be a strategic asset for the company, and how it is possible to mix curiosity-driven discovery with invention by the proper choice of research area.

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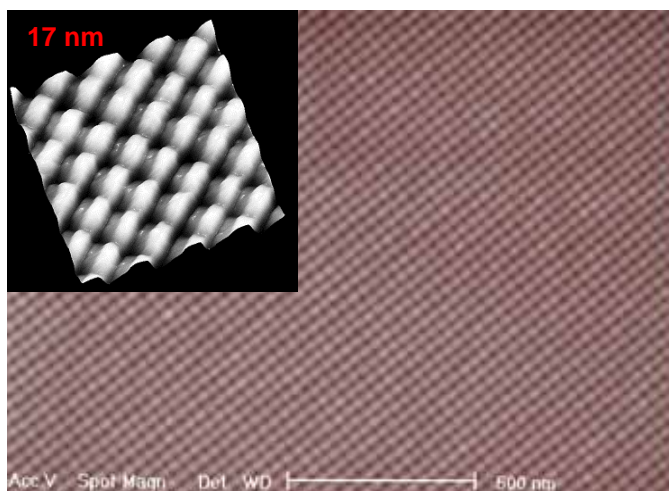
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### Figure:



(Right) A scanning electron micrograph of the central region of a 13,000 junction metal cross-bar structure fabricated at a half-pitch of 17 nm using the process of imprint lithography. The inset shows an atomic force microscopy (AFM) topograph of a magnified region of the cross-bar. This simple structure is the basis for both high density memory and logic circuits.